ANCORA
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# Thermal Management for GaNFET Device

Rev. 01

# 1. Structure of GaN packaging

The GaN-FET devices, as shown in Figure 1, exhibit two kinds of heat dissipation path.

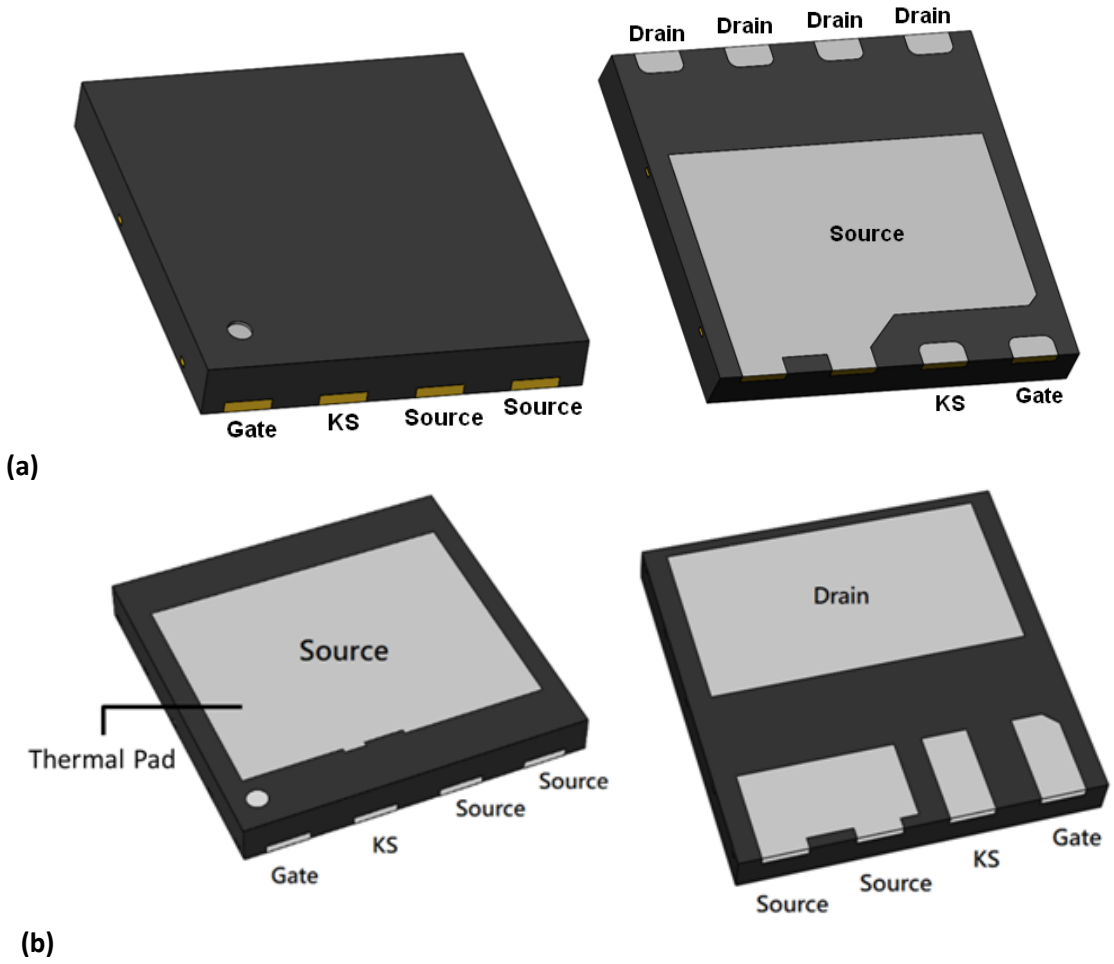


**Figure 1 (a) Bottom side cooled device ; (b) Double side cooled device**

1.1 Bottom side cooled device

Wire bond is used to connect chip and lead frame. Wire bonding is generally considered the most cost-effective and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages.

1.2 Double side cooled device

Flip chip technology is used to connect chip with lead frame. One thermal pad on the top side of device can be connected to heatsink.

## 2. Thermal resistance definition

According to the definition in JESD51-1, the thermal resistance of a semiconductor device is generally defined as:

$$R_{thJX} = \frac{T_J - T_X}{P_H} \quad (1)$$

Where $R_{thJX}$ = thermal resistance from device junction to the specific reference point [°C/W].

$T_J$ = device junction temperature in the steady state test condition [°C]

$T_X$ = reference temperature for the specific location [°C]

$P_H$ = power dissipated in the device [W]

### 2.1 Device only: Junction-to-case thermal resistance ($R_{thJC}$)

Thermal resistance is the measure of a package's heat dissipation capability from a die's active surface (junction) to a specified reference point (case). Reference points here are selected as case_top and case_bottom according to the two main heat dissipation paths. $R_{thJC}$ is defined as "top side ($R_{thJC\_top}$)" and "bottom side ($R_{thJC\_bottom}$)" respectively.

#### 2.1.1 Bottom side cooled device

The device is encapsulated with epoxy mold compound (EMC), which is the poor conductor of thermal. Therefore, the device is not recommended to dissipate heat from the top side. The specified reference point (case_bottom) is selected below the chip and the lead frame, as shown in Figure 2.

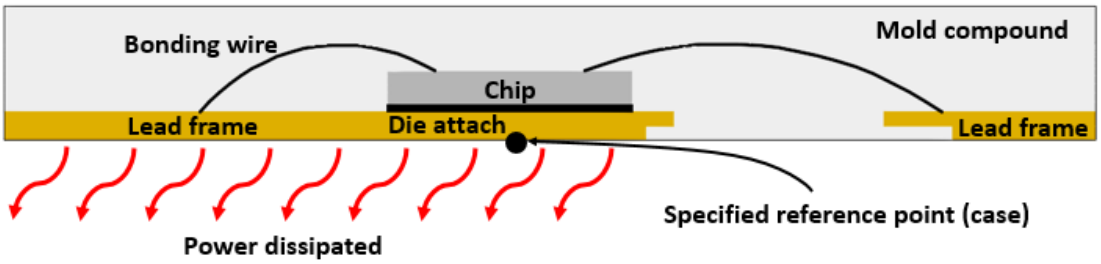


**Figure 2 Cross-section view of bottom side cooled device.**

2.1.2 Double side cooled device

The exposed thermal pad is connected electrically to the source and can be used to dissipate heat. There are two reference points in this device structure which are selected as case_top and case_bottom, as shown in Figure 3.

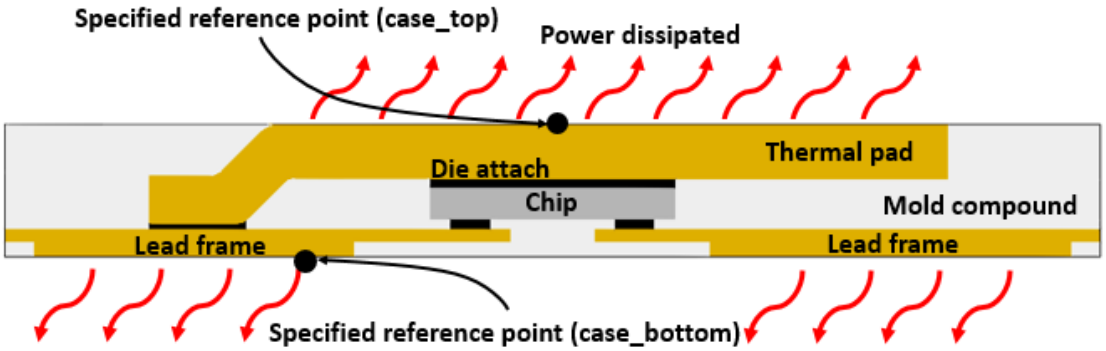


**Figure 3 Cross-section view of double side cooled device.**

2.2 Real System : Junction-to-ambient thermal resistance ( $R_{thJA}$)

As described in the JESD51-1, the thermal resistance of a semiconductor device is generally defined as equation 1. When the specific location is ambient, therefore $T_A = T_X$, the $R_{thJA}$ equation:

$$R_{thJA} = \frac{T_J - T_A}{P_H} \qquad (2)$$

# 3. Thermal management for device

## 3.1 Impact of thermal via pattern

Thermal via provide better thermal paths within PCB to improve heat transfer from the device to the ambient or cooling system. To find out the effects of heat transfer by increasing the pattern area of thermal via in the PCB, $R_{thJA}$ simulations versus the pattern area of thermal via in the inner PCB layer is completed.

For putting vias directly in the SMT pads, resin filled via was recommended.

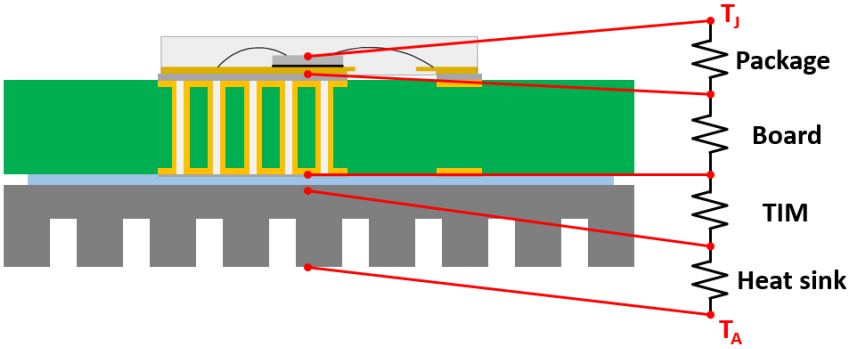


**Figure 4 Thermal network of simulation model.**

The device is mounted on the center of the PCB, and the PCB dimension is 30 x 66 x 1.6 mm. Figure 4 shows an equivalent thermal network for the device on PCB with a heatsink below. The heat flow from junction, where the heat is generated, passes through device, board, TIM, heatsink to the ambient.

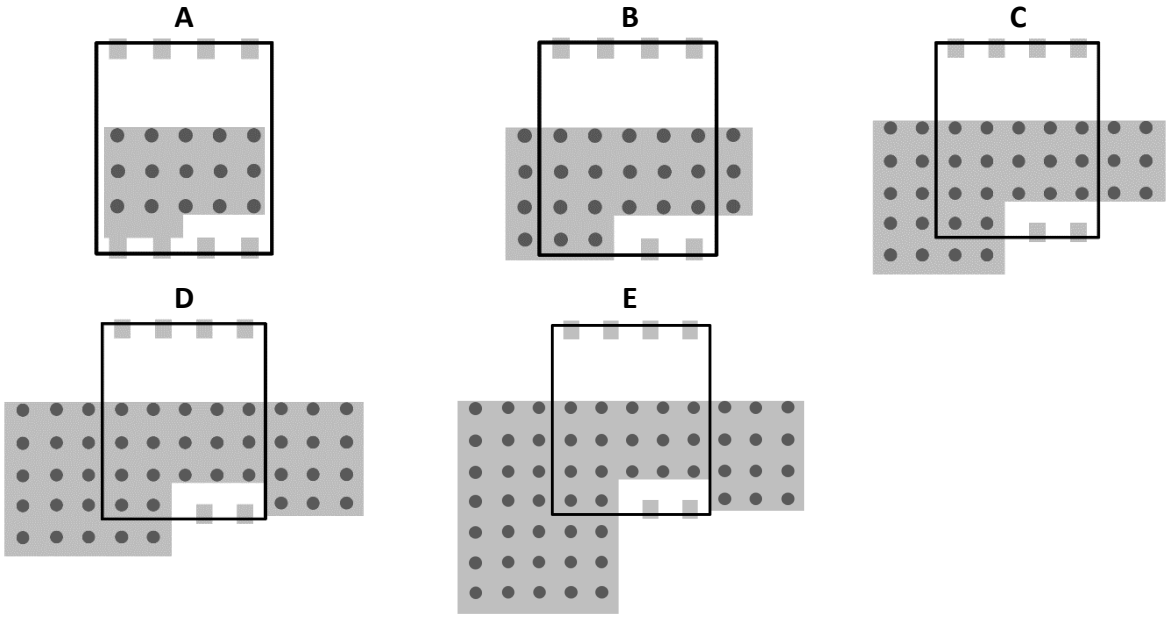


**Figure 5 Different layouts for $R_{th\text{-}JA}$ simulations on heat transfer effects.**

Figure 5 shows five different patterns for the same device (FET-E60300B010), which vary in pattern area and number of thermal via. Thermal via parameters are as follows: diameter=0.4mm, via is filled with resin, wall thickness= 30µm, pitch= 1mm, and via number 15/24/35/46/56 respectively.

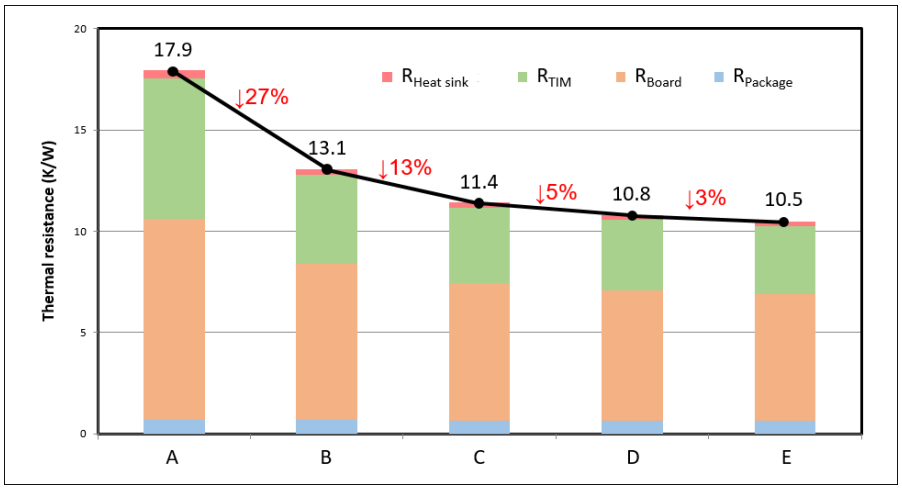


**Figure 6 Simulated $R_{th}$ of each pattern.**

As shown in Figure 6, the $R_{th}$ vary more than 40% from A to C. This means more via distributed within 2mm around the footprint of this device would have a big influence on the thermal resistance.

## 3.2 Bottom side cooling

It's suggested that the PCB footprint can be designed with appropriate thermal via pattern. Heat can then effectively be transferred to the other side of the PCB. TIM and heatsink can be added on the other side of the PCB for better heat dissipation. Please refer to Figure 4 for the detailed structure.

3.3 Double side cooling

Double side cooled device is designed for cooling from both thermal pad and the footprint simultaneously. Thermal pad plays an important role for the heat conduction from the internal die (Junction) to the top surface of the device effectively. By attaching a TIM (Thermal Interface Material) and heatsink on thermal pad, one additional heat path besides bottom side is created, as shown in Figure 7. The cooling system on the bottom side (footprint) can refer to bottom side cooling.

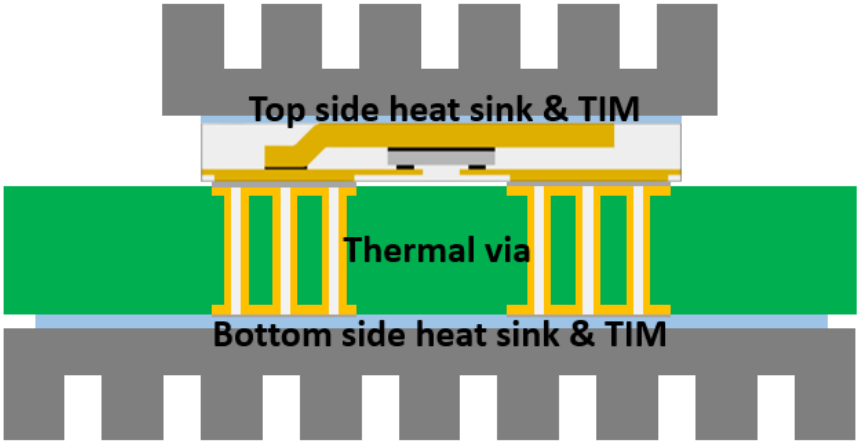


**Figure 7 Thermal system of double side cooled package**

## Revision History

| Revision | Date | Description of Change |
|---|---|---|
| 00 | 2021-01-07 | First Release |
| 01 | 2021-03-24 | Fix the typo |
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